In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) A method for dynamic adjustment of priority and step procedures for determining effective lot dispatching for wafer and chip probing, comprising:

A. using a two-phased, event-driven dispatching system structure, comprising lot rank and lot assignment, for said dynamic adjustment, wherein said lot rank comprises a lot rank priority formula for production wafers and packages, and a lot rank for engineering lots, and wherein said priority formula of:

Priority = Σ (Base*Weight_x) calculates priority;

B. using said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;

C. providing for engineering lots capacity check in said step procedures;

D. solving dispatching conflict between wafer and package lots, and

E. limiting tester's capability in product through use of common constraint system.

2. – 4. (canceled)

5. (currently amended) The method for dynamic adjustment of priority and step procedures of claim [[2]] 1, wherein said lot assignment [[to]] comprises [[of]] exception lots, hot run, super

hot run, normal lot, and engineering lot dispatching rule with the object [[of]] being based on Master Production Schedule target to reduce setup time.

6. (original) The method for dynamic adjustment of priority and step procedures of claim 1, wherein dispatch in a test foundry can be affected by performance indices, special dispatch properties, auxiliary apparatus, tester constraints, and production mode.

7. (original) The method for dynamic adjustment of priority and step procedures of claim 1, wherein said auxiliary apparatus includes tester, probe card, and load board.

8. (currently amended) A [[The]] method for dynamic adjustment of priority and step procedures ~~of claim 1~~ for determining effective lot dispatching for wafer and chip probing, comprising:

A. using a two-phased, event-driven dispatching system structure for said dynamic adjustment;

B. using said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;

C. providing for engineering lots capacity check in said step procedures;

D. solving dispatching conflict between wafer and package lots, and

E. limiting tester's capability in product through use of common constraint system,

wherein a multi-priority factor and multi-dispatching step procedure is enhanced to fit complex dispatching demands of a test foundry and used with ~~different operation types such as~~ chip probing and final testing.

9. (currently amended) A [[The]] method for dynamic adjustment of priority and step procedures ~~of claim 1~~ for determining effective lot dispatching for wafer and chip probing, comprising:

A. using a two-phased, event-driven dispatching system structure for said dynamic adjustment;

B. using said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;

C. providing for engineering lots capacity check in said step procedures;

D. solving dispatching conflict between wafer and package lots, and

E. limiting tester's capability in product through use of common constraint system,

wherein said method is based on distinct production goals or behavior reported by production and engineering devices to in real time get the most desirable dispatching list for a particular tester at any given time.

10. (original) The method for dynamic adjustment of priority and step procedures of claim 1, wherein said step procedures are expanded to consider different product lots in addition to same products to said utilize any same said auxiliary apparatus without need for new set up.

11. (currently amended) A [[The]] method for dynamic adjustment of priority and step procedures ~~of claim 1~~ for determining effective lot dispatching for wafer and chip probing, comprising:

A. using a two-phased, event-driven dispatching system structure for said dynamic adjustment;

B. using said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;

C. providing for engineering lots capacity check in said step procedures;

D. solving dispatching conflict between wafer and package lots, and

E. limiting tester's capability in product through use of common constraint system,

wherein said engineering lot capacity limitation check is done to see if the amount of fixed testing time per week determined by testing site personnel for engineering lots to be tested on any particular machine has been exceeded.

12. (original) The method for dynamic adjustment of priority and step procedures of claim 11, wherein said engineering lots are dispatched automatically with manual effort only needed for setting exception rules and taking care of special cases thereby eliminating need for manual dispatching sheet.

13. (original) The method for dynamic adjustment of priority and step procedures of claim 1, wherein said dispatching conflict between wafer and package lots is avoided by having said step procedures make sure no wafer work in progress remains before allowing said package lots to be dispatched with the result of minimal changeovers.

14. (original) The method for dynamic adjustment of priority and step procedures of claim 13, wherein said package lots are treated as an engineering step procedure with a added considerations of dispatching a same product or same production type as a lot just tested and resource constraint of a load board.

15. (original) The method for dynamic adjustment of priority and step procedures of claim 1, wherein said common constraint system is a PROMIS constraint system.

16. (currently amended) A [[The]] method for dynamic adjustment of priority and step procedures ~~of claim 15~~ for determining effective lot dispatching for wafer and chip probing, comprising:

A. using a two-phased, event-driven dispatching system structure for said dynamic adjustment;

B. using said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;

C. providing for engineering lots capacity check in said step procedures;

D. solving dispatching conflict between wafer and package lots, and

E. limiting tester's capability in product through use of common constraint system, wherein said common constraint system is a PROMIS constraint system, and

wherein said PROMIS constraint system provides a function for users to limit said tester's product capability from which said step procedure's last step is to check said PROMIS constraint system to filter out inappropriate lots to avoid mistake operations.

17. (currently amended) A system for dynamic adjustment of priority and step procedures for determining effective lot dispatching for wafer and chip probing, comprising:

a means to use a two-phased, event-driven dispatching system structure for said dynamic adjustment, wherein said two-phased, event-driven dispatching system structure comprises lot rank and lot assignment, said lot rank comprises of a lot rank priority

formula for production wafers and packages and a lot rank for engineering lots, and wherein said priority formula of:

$\underline{\text{Priority} = \Sigma (\text{Base} * \text{Weight}_x) \text{ calculates priority;}}$

a means to use said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;

a means to provide engineering lots capacity check in said step procedures;

a means to solve dispatching conflict between wafer and package lots, and

means to limit tester's capability in product through constraint.

18. – 20. (canceled)

21. (currently amended) The system for dynamic adjustment of priority and step procedures of claim [[18]] 17, wherein said lot assignment to comprises of exception lots, hot run, super hot run, normal lot, and engineering lot dispatching rule with the object of being based on Master Production Schedule target to reduce setup time.

22. (original) The system for dynamic adjustment of priority and step procedures of claim 17, wherein dispatch in a test foundry can be affected by performance indices, special dispatch properties, auxiliary apparatus, tester constraints, and production mode.

23. (original) The system for dynamic adjustment of priority and step procedures of claim 17, wherein said auxiliary apparatus includes tester, probe card, and load board.

24. (currently amended) A [[The]] system for dynamic adjustment of priority and step procedures ~~of claim 17~~ for determining effective lot dispatching for wafer and chip probing, comprising:

a means to use a two-phased, event-driven dispatching system structure for said dynamic adjustment,

a means to use said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;

a means to provide engineering lots capacity check in said step procedures;

a means to solve dispatching conflict between wafer and package lots, and

means to limit tester's capability in product through constraint, wherein a multi-priority factor and multi-dispatching step procedure is enhanced to fit complex dispatching demands of a test foundry and used with ~~different operation types such as~~ chip probing and final testing.

25. (currently amended) A [[The]] system for dynamic adjustment of priority and step procedures ~~of claim 17~~ for determining effective lot dispatching for wafer and chip probing, comprising:

a means to use a two-phased, event-driven dispatching system structure for said dynamic adjustment,

a means to use said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;

a means to provide engineering lots capacity check in said step procedures;

a means to solve dispatching conflict between wafer and package lots, and

means to limit tester's capability in product through constraint,

wherein based on distinct production goals or behavior reported by production and engineering devices to in real time get the most desirable dispatching list for a particular tester at any given time.

26. (original) The system for dynamic adjustment of priority and step procedures of claim 17, wherein said step procedures are expanded to consider different product lots in addition to same products to said utilize any same said auxiliary apparatus without need for new set up.

27. (currently amended) A [[The]] system for dynamic adjustment of priority and step procedures ~~of claim 17~~ for determining effective lot dispatching for wafer and chip probing, comprising:

a means to use a two-phased, event-driven dispatching system structure for said dynamic adjustment,

a means to use said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup;

a means to provide engineering lots capacity check in said step procedures;

a means to solve dispatching conflict between wafer and package lots, and

means to limit tester's capability in product through constraint,

wherein said engineering lot capacity limitation check is done to see if the amount of fixed testing time per week determined by testing site personnel for engineering lots to be tested on any particular machine has been exceeded.

28. (original) The system for dynamic adjustment of priority and step procedures of claim 27, wherein said engineering lots are dispatched automatically with manual effort only needed for setting exception rules and taking care of special cases thereby eliminating need for manual dispatching sheet.

29. (original) The system for dynamic adjustment of priority and step procedures of claim 17, wherein said dispatching conflict between wafer and package lots is avoided by having said step procedures make sure no wafer work in progress remains before allowing said package lots to be dispatched with the result of minimal changeovers.

30. (currently amended) The system for dynamic adjustment of priority and step procedures of claim 29, wherein said package lots are treated as an engineering step procedure with [[the]] added considerations of dispatching [[the]] same product or same production type as [[the]] a lot just tested and resource constraint of [[said]] a load board.

31. (currently amended) The system for dynamic adjustment of priority and step procedures of claim 17, wherein [[said]] a common constraint system is [[the]] a PROMIS constraint system.

32. (original) The system for dynamic adjustment of priority and step procedures of claim 31, wherein said PROMIS constraint system provides a function for users to limit said tester's product capability from which said step procedure's last step is to check said PROMIS constraint system to filter out inappropriate lots to avoid mistake operations.